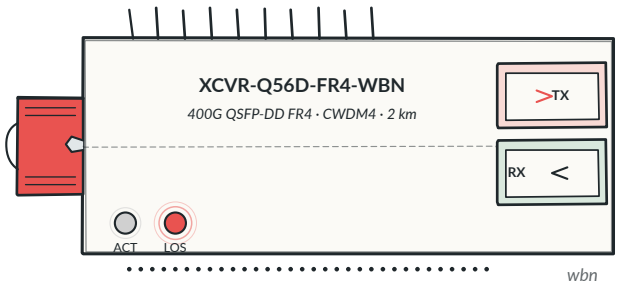
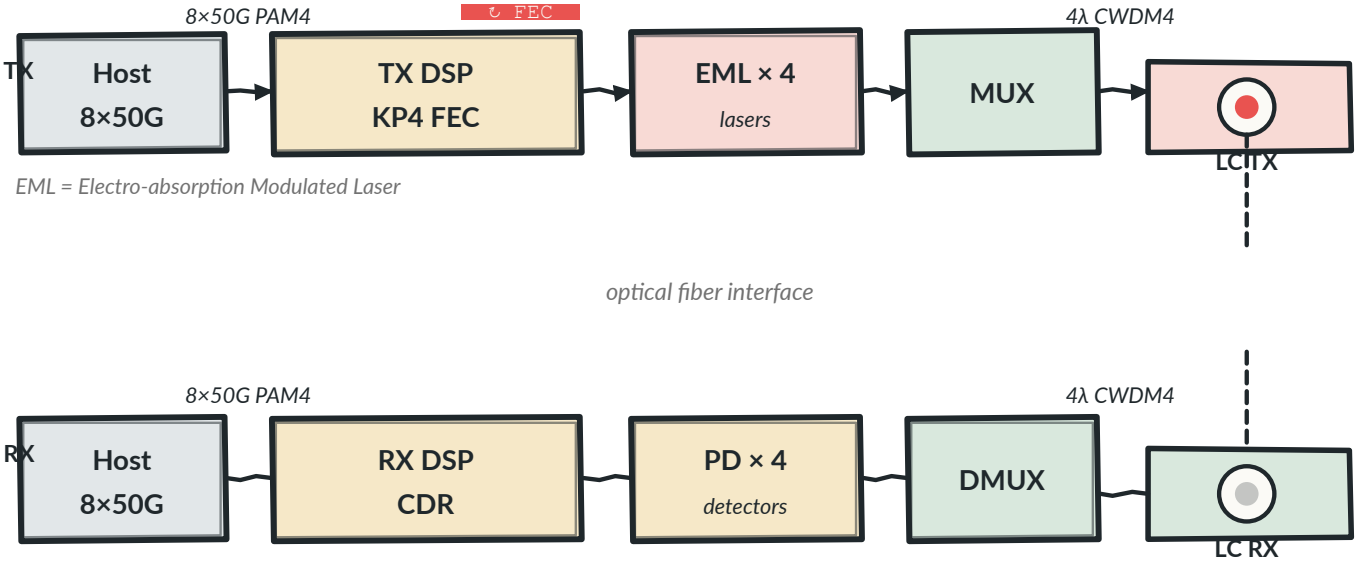
MODULE



KEY FACTS

Form factor	QSFP-DD
Standard	IEEE 802.3cu 400GBASE-FR4
Wavelength plan	4λ CWDM4 (1271 / 1291 / 1311 / 1331 nm)
Reach	≤ 2 km, OS2 SMF
TX power range	−6 / 4.5 dBm
FEC	RS(544,514) KP4
Management	CMIS 5.x
Temperature	Commercial (0 °C to 70 °C)

BLOCK DIAGRAM



TRANSMITTER OPTICAL — PER LANE

Lane	λ (nm)	Min (dBm)	Max (dBm)
0	1271	−3.2	4.4
1	1291	−3.2	4.4
2	1311	−3.2	4.4
3	1331	−3.2	4.4

RECEIVER OPTICAL — PER LANE

Lane	λ (nm)	Min (dBm)	Max (dBm)
0	1271	−7.2	4.4
1	1291	−7.2	4.4
2	1311	−7.2	4.4
3	1331	−7.2	4.4

WAVELENGTH PLAN

1271 nm	1291 nm	1311 nm	1331 nm
Lane 0	Lane 1	Lane 2	Lane 3

CWDM4 wavelength plan per IEEE 802.3cu Table 138-7. Colors are perceptual placeholders; actual wavelengths are SWIR (invisible).

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Supply Voltage	-0.5	3.6	V
Damage Threshold, each lane	5.4	—	dBm

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Unit
Supply Voltage	-0.5	—	3.6	V
Power Supply Voltage	3.135	3.3	3.465	V

TX PERFORMANCE MARGIN

TX AVG POWER	IEEE 802.3cu envelope	headroom
−3.2 / 4.4 dBm	−6 / 4.5 dBm	**2.8 / 0.1 dB**

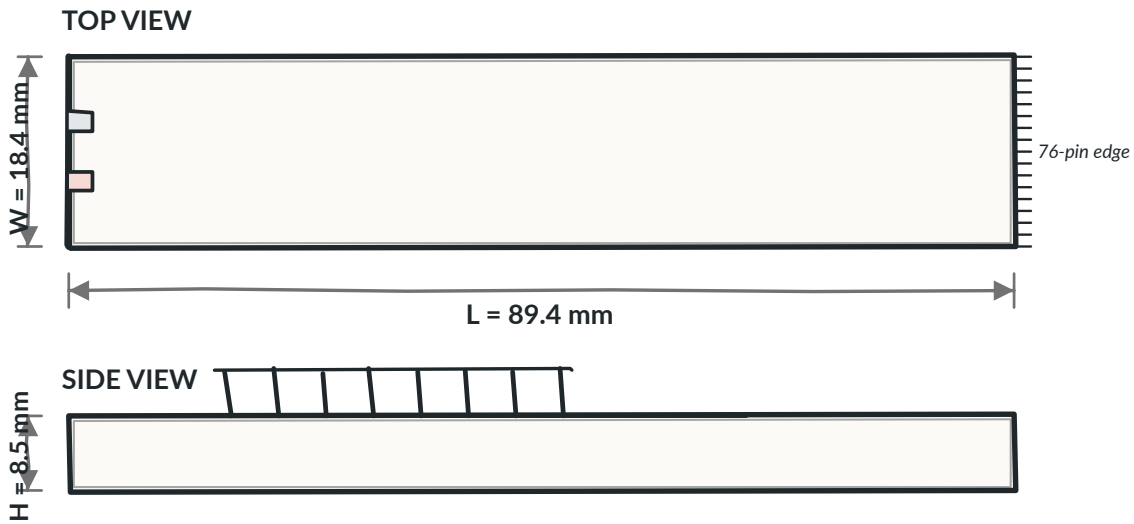
RX PERFORMANCE MARGIN

RX RANGE	IEEE 802.3cu envelope	headroom
−7.2 / 4.4 dBm	−10 / 4.5 dBm	**2.8 / 0.1 dB**

DIGITAL DIAGNOSTICS (CMIS 5.X)

Parameter	Min	Typ	Max	Unit
Temperature (DDM)	0	±3	70	°C
Voltage (DDM)	—	0.1	—	V
Tx Bias Current Each Lane (DDM)	0	10%	100	mA
Tx Output Power Each Lane (DDM monitor accuracy)	-3.2	±3	+4.4	dB
Rx Receive Power Each Lane (DDM monitor accuracy)	-7.2	±3	+4.4	dB

MECHANICAL



76-pin dual-row edge contact · 0.75 mm pitch · QSFP-DD MSA Rev 5.0

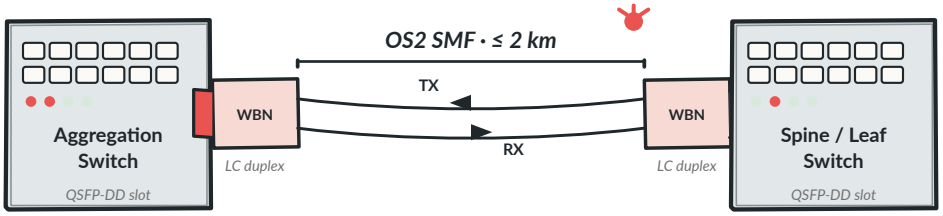
all dimensions ± 0.1 mm unless noted

HOST-BOARD PINOUT (QSFP-DD MSA)

Pin	Sym	Description
1	GND	Ground
2	Tx2-	Transmitter inverted data input, lane 2
3	Tx2+	Transmitter non-inverted data input, lane 2
4	GND	Ground
5	Tx4-	Transmitter inverted data input, lane 4
6	Tx4+	Transmitter non-inverted data input, lane 4
7	GND	Ground
8	ModSelL	Module Select, active low
9	ResetL	Module Reset, active low
10	VccRx	+3.3V power supply receiver
11	SCL	2-wire serial interface clock
12	SDA	2-wire serial interface data
13	GND	Ground
14	Rx3+	Receiver non-inverted data output, lane 3
15	Rx3-	Receiver inverted data output, lane 3
16	GND	Ground
17	Rx1+	Receiver non-inverted data output, lane 1
18	Rx1-	Receiver inverted data output, lane 1
19	GND	Ground
20	GND	Ground
21	Rx2-	Receiver inverted data output, lane 2
22	Rx2+	Receiver non-inverted data output, lane 2
23	GND	Ground
24	Rx4-	Receiver inverted data output, lane 4
25	Rx4+	Receiver non-inverted data output, lane 4
26	GND	Ground
27	ModPrsL	Module Present, active low
28	IntL	Interrupt, active low
29	VccTx	+3.3V power supply transmitter
30	Vcc1	+3.3V power supply
31	InitMode	Initialization mode (called LPMODE in legacy QSFP applications)
32	GND	Ground
33	Tx3+	Transmitter non-inverted data input, lane 3
34	Tx3-	Transmitter inverted data input, lane 3
35	GND	Ground
36	Tx1+	Transmitter non-inverted data input, lane 1
37	Tx1-	Transmitter inverted data input, lane 1
38	GND	Ground

Pin	Sym	Description
39	GND	Ground
40	Tx6-	Transmitter inverted data input, lane 6
41	Tx6+	Transmitter non-inverted data input, lane 6
42	GND	Ground
43	Tx8-	Transmitter inverted data input, lane 8
44	Tx8+	Transmitter non-inverted data input, lane 8
45	GND	Ground
46	Reserved	Reserved for future use
47	VS1	Module vendor specific 1
48	VccRx1	+3.3V power supply (receiver, second row)
49	VS2	Module vendor specific 2
50	VS3	Module vendor specific 3
51	GND	Ground
52	Rx7+	Receiver non-inverted data output, lane 7
53	Rx7-	Receiver inverted data output, lane 7
54	GND	Ground
55	Rx5+	Receiver non-inverted data output, lane 5
56	Rx5-	Receiver inverted data output, lane 5
57	GND	Ground
58	GND	Ground
59	Rx6-	Receiver inverted data output, lane 6
60	Rx6+	Receiver non-inverted data output, lane 6
61	GND	Ground
62	Rx8-	Receiver inverted data output, lane 8
63	Rx8+	Receiver non-inverted data output, lane 8
64	GND	Ground
65	NC	No connect (must be left unconnected within module)
66	Reserved	Reserved for future use
67	VccTx1	+3.3V power supply (transmitter, second row)
68	Vcc2	+3.3V power supply (second row)
69	Reserved	Reserved for future use
70	GND	Ground
71	Tx7+	Transmitter non-inverted data input, lane 7
72	Tx7-	Transmitter inverted data input, lane 7
73	GND	Ground
74	Tx5+	Transmitter non-inverted data input, lane 5
75	Tx5-	Transmitter inverted data input, lane 5
76	GND	Ground

APPLICATION TOPOLOGY



400G QSFP-DD FR4 · CWDM4 · point-to-point · data center interconnect

COMPLIANCE & STANDARDS

- IEEE 802.3cu 400GBASE-FR4
- QSFP-DD MSA Rev 5.0
- CMIS 5.x
- RoHS 2011/65/EU
- CE
- FCC Class A

ORDERING INFORMATION

Part number	Description
XCVR-Q56D-FR4-WBN	400G QSFP-DD FR4, 2 km, commercial temperature

HANDLING & STORAGE

- ESD: Class 1B HBM (500 V), Class M1 MM (100 V); handle per ESD S20.20.
- Storage: -40 °C to +85 °C, ≤ 95 % RH non-condensing.
- Install and remove using the pull-tab. Do not hot-plug without latch engagement.
- Clean the optical connector per IEC 61300-3-35 prior to mating.

REVISION HISTORY

Rev	Date	Description
1.0	2026-05-13	Initial publication

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Datasheet
XCVR-Q56D-FR4-WBN · Rev 1.0

All specifications are subject to change without notice. Performance figures assume IEEE 802.3cu-compliant host and KP4 FEC.